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Multifunctional high-performance van der Waals heterostructures

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A range of novel two-dimensional materials have been actively explored for More Moore and More-than-Moore device applications because of their ability to form van der Waals heterostructures with unique electronic properties. However, most of the reported electronic devices exhibit insufficient control of multifunctional operations. Here, we leverage the band-structure alignment properties of narrow-bandgap black phosphorus and large-bandgap molybdenum disulfide to realize vertical heterostructures with an ultrahigh rectifying ratio approaching 10^6 and on–off ratio up to 10^7. Furthermore, we design and fabricate tunable multivalue inverters, in which the output logic state and window of the mid-logic can be controlled by specific pairs of channel length and, most importantly, by the electric field, which shifts the band-structure alignment across the heterojunction. Finally, high gains over 150 are achieved in the inverters with optimized device geometries, showing great potential for future logic applications.

Two-dimensional (2D) materials offer a unique opportunity for the integration of heterogeneous systems due to the weak van der Waals interactions between individual layers, without dangling bonds on the surfaces. It is therefore possible to easily assemble different 2D materials into functional devices without the restraint of lattice mismatch and the need for the sophisticated and sometimes impractical growth procedures required for fabrication of conventional heterojunctions[1,2]. Various van der Waals heterostructures have been demonstrated, including tunnelling field-effect transistors based on a graphene/BN/graphene structure[3], vertical field-effect transistors (VFETs)[4–6] and optoelectronic devices with the integration of transition-metal dichalcogenides (TMDCs)[7–15]. However, much less has been reported regarding heterostructures based on black phosphorus (BP), another recently rediscovered 2D material, which exhibits high hole mobility and, unlike many other 2D materials, has a direct bandgap[16–23]. In heterostructures, rectifying characteristics rely mainly on the Fermi level modulation of the channel, and the band-structure offset of the conduction band minimum and valence band maximum identifies where electrons and holes can be accumulated or depleted from quantum wells. Previous studies on such vertical heterostructures suggest that the combination of high rectifying ratio and on–off ratio, which is desirable for logic applications, is hard to achieve[4–6,24]. These issues are usually limited by the intrinsically smaller barriers in graphene–TMDC junctions and the lack of a bandgap offset that can induce a potential well for carrier reservation. BP is an unintentionally p-doped narrow-bandgap semiconductor[22,23], and MoS_2 is a large-bandgap n-type semiconductor with reasonably high electron mobility[25–27]. The combination of these materials provides a large bandgap offset, achieving both a high on–off ratio and good rectifying characteristics. Moreover, the electron affinity difference for these materials is only 0.1 eV (refs 28–30), which opens the possibility of tuning the energy band offset. By changing the bias and therefore the channel Fermi level, a transition from a conventional binary inverter to a ternary inverter has been observed. The position and range of the middle logic values can be tuned via the bias voltage and channel lengths in this device, so its multifunctionality and high tunability exceeds previous binary logic devices based on 2D semiconductors[30–40]. Due to the higher number of logic states and higher data storage density, ternary logic is considered to be a promising alternative to traditional binary logic[15,41]. Nevertheless, systematic studies of such logic devices based on 2D semiconductors are largely lacking.

In the first part of this work, we systemically study the electronic transport properties of BP/MoS_2-based heterojunctions, especially in relation to band alignment modulation. In the vertical structure device, where a high-performance diode and FET are integrated into a single device, we obtain a record-high current rectification ratio ($\sim 1 \times 10^6$) and high on–off ratio (1×10^7) simultaneously, with a large current density ($>1 \times 10^3$ A cm^{-2}). We then focus on MoS_2–BP heterostructure-based logic devices by engineering the partition load and matching, and successfully demonstrate the first tunable ternary inverter, in which both the middle output value and middle region length can be controlled. Finally, by optimizing the channel length of the individual BP and MoS_2 FETs, we demonstrate a high-performance binary inverter with a record high gain of over 150. We also perform an air-stability study with encapsulation and investigate the temperature dependence of the above functional devices from room temperature down to 20 K. With a thin Al_2O_3 cap layer formed from a 3 nm Al layer deposited by physical vapour deposition (PVD), the BP devices exhibit air-stable device performance for up to 8 weeks, without any sign of further degradation.

To fully explore electronic transport in BP/MoS_2-based heterojunctions, we designed and fabricated various hybrid structures, including chemical vapour deposited (CVD) MoS_2–BP and exfoliated multilayer MoS_2–BP heterostructures, as shown in Fig. 1a and b, respectively. Raman measurements on the overlap region were taken, as shown in Fig. 1c,d (with top layers of BP and MoS_2, respectively). In both cases, the five peaks (black, BP peaks; red, MoS_2 peaks) are consistent with previous studies[28]. Photoluminescence measurements on monolayer MoS_2 are presented in the inset of Fig. 1c. The peak position is at 673 nm and the half-peak width is 23 nm, indicating good quality of the thin film[42]. These different structures are the basis for the various functional BP–MoS_2 heterojunction devices and inverters described in the following sections.

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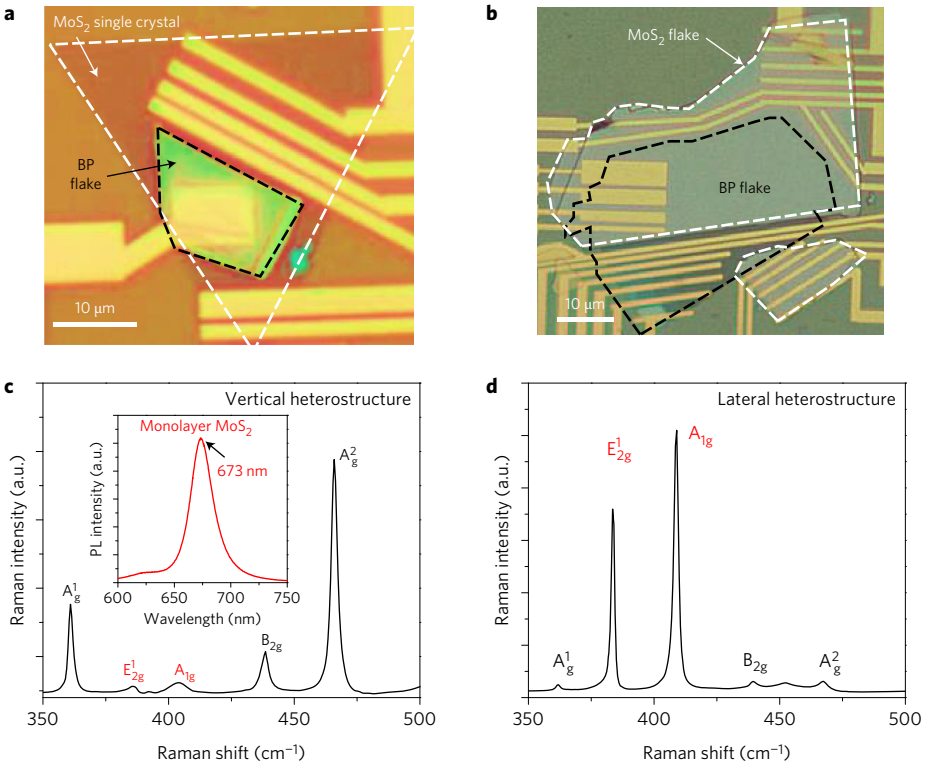


Figure 1 | Heterostructure schematics and material characterization. a,**b**, Optical microscopic images of BP and MoS_2 heterostructures using single-layer CVD MoS_2 (**a**) and exfoliated multilayer MoS_2 (**b**). Scale bars, 10 μm. **c**, Raman characterization in the heterojunction overlapped region, in which the top layer is a BP flake. Inset: photoluminescence (PL) measurement of the single-layer CVD MoS_2. **d**, Raman characterization in the heterojunction overlapped region, in which the top layer is MoS_2 flake.

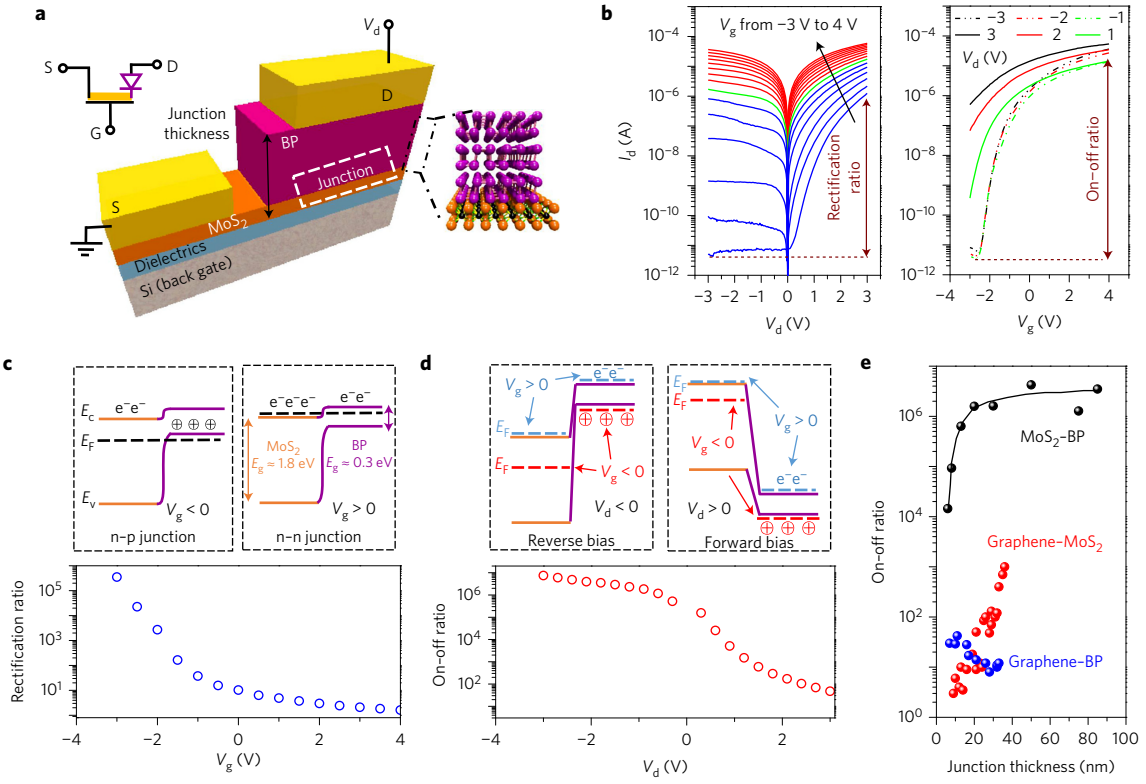


Figure 2 | Electronic properties of VFET. a, Schematic view of the VFET. **b**, I_d–V_d output characteristics and I_d–V_g transfer characteristics of the device in semilogarithmic scale. **c**, Energy band diagrams and rectification ratio at different gate voltages. **d**, Energy band diagrams and on–off ratio at different drain voltages. **e**, Comparison of on–off ratio for different materials systems in VFET structures. Reference data are sourced from this work (MoS_2–BP), ref. 4 (graphene–MoS_2) and ref. 24 (graphene–BP), respectively.

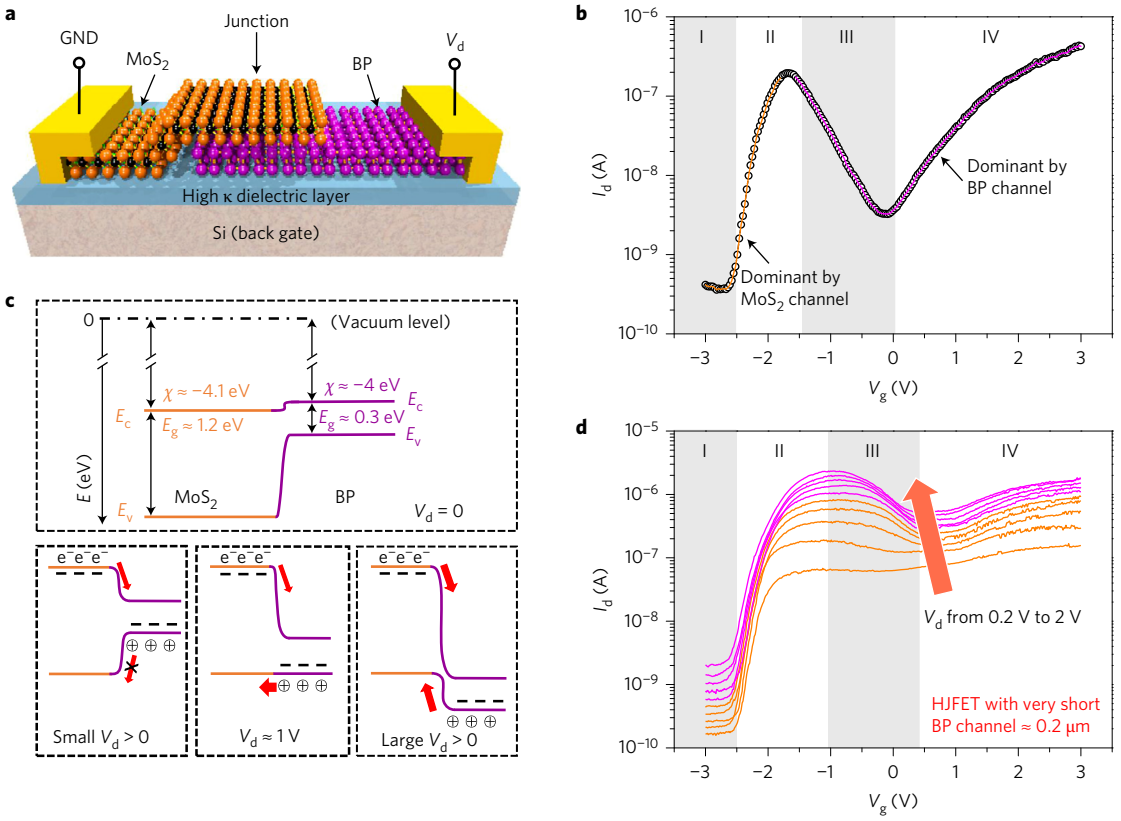


Figure 3 | Electronic properties of the lateral HJFET. a, Schematic view of the lateral HJFET. **b**, Transfer characteristics in four regions of a typical BP/MoS_2-based heterostructure, in which the drain voltage is 1 V. **c**, Energy band diagrams at different bias conditions. The bandgap of multilayer MoS_2 is ~1.2, and is 0.3 eV for the BP flake. **d**, I_d-V_g curves of the lateral HJFET with a short BP channel of 0.2 μm. The peak-to-valley ratio in region III becomes larger as V_d increases from 0.2 to 2 V.

VFET

As shown in Fig. 2a, the vertical heterojunction consists of a BP channel on top of a MoS_2 layer. Current flows between the bottom electrode and top metal electrode, passing through the semiconducting BP channel. The thickness of this channel is designated as the channel length in some literature, but here we define the carrier injection path as the junction thickness[4,6]. This heterojunction integrates a high-performance diode and a FET as a single structure. Its electric transport characteristics are presented in Fig. 2b, where the left and right panels represent the output and transfer characteristics, respectively. Well-behaved rectifying behaviour can be achieved simultaneously with a large on–off ratio. For instance, the device has a rectification ratio of $\sim 4 \times 10^5$ (current at $V_d = 3$ V versus current at $V_d = -3$ V) at $V_g = -3$ V, and an on–off ratio of up to 1×10^7 (current at $V_g = 4$ V versus current at $V_g = -3$ V) at $V_d = -3$ V.

To better understand the mechanisms, we plot the rectification ratio versus V_g and on–off ratio versus V_d in Fig. 2c,d, together with the band alignment. The rectification ratio decreases rapidly as the gate voltage increases. Under negative V_g, holes accumulate greatly in the BP flake, while the MoS_2 sheet remains n-type due to the Fermi pinning effect[27]. As a result, a PN heterojunction is formed and the device shows diode-like rectifying characteristics. While under positive V_g, the device is doped as an n–n junction because of the ambipolar nature of BP, and it shows ohmic-like behaviour with rectification ratio close to 1. On the other hand, the on–off ratio decreases when the drain voltage changes from reverse bias to forward bias. Under reverse bias, the built-in potential is increased and a p–n heterojunction is formed at $V_g < 0$ (red symbols), which results in a very small current. Meanwhile, an n–n junction is formed at $V_g > 0$ (blue symbols), which results in large current, regardless of the reverse junction bias, leading to a large on–off ratio. While under forward bias, the quasi-Fermi-level difference generates excess minority carriers in the depletion region, which diffuse through the junction, and current is always large in the entire range of V_g. As a comparison, the on–off ratios of such vertical heterojunctions based on different materials are summarized in Fig. 2e[4,24]. Using band alignment engineering of van der Waals heterostructures based on BP and MoS_2, our device shows better performance than counterparts reported in previous studies[4–6,24] (Supplementary Section 1).

Lateral heterojunction FET

A lateral heterojunction FET (HJFET) structure, in which the two electrodes are separately located on a BP flake and MoS_2 sheet, away from the overlapped junction region, has also been demonstrated (Fig. 3a). Electrons are injected from the source to drain electrode through the MoS_2 channel, the heterojunction and BP channel, consecutively. The global gate controls the entire channel electrostatic potential, resulting in non-monotonic current modulation due to the non-uniformity of the channel[10,15]. The transfer characteristics are plotted in Fig. 3b, where the drain is at forward bias for the p–n heterojunction. Electric current transport can be sorted into four regions. In region I ($V_g < -2.5$ V), the MoS_2 channel is fully depleted, which turns off the entire channel and results in the smallest I_d. In region II (-2.5 V $< V_g < -1.5$ V), the gate bias starts to turn in both the non-overlapped MoS_2 channel region and the MoS_2 region in the heterojunction. In region III (-1.5 V $< V_g < 0$ V), when the heterojunction is fully turned on, the drain current will be dominated by the non-overlapped BP

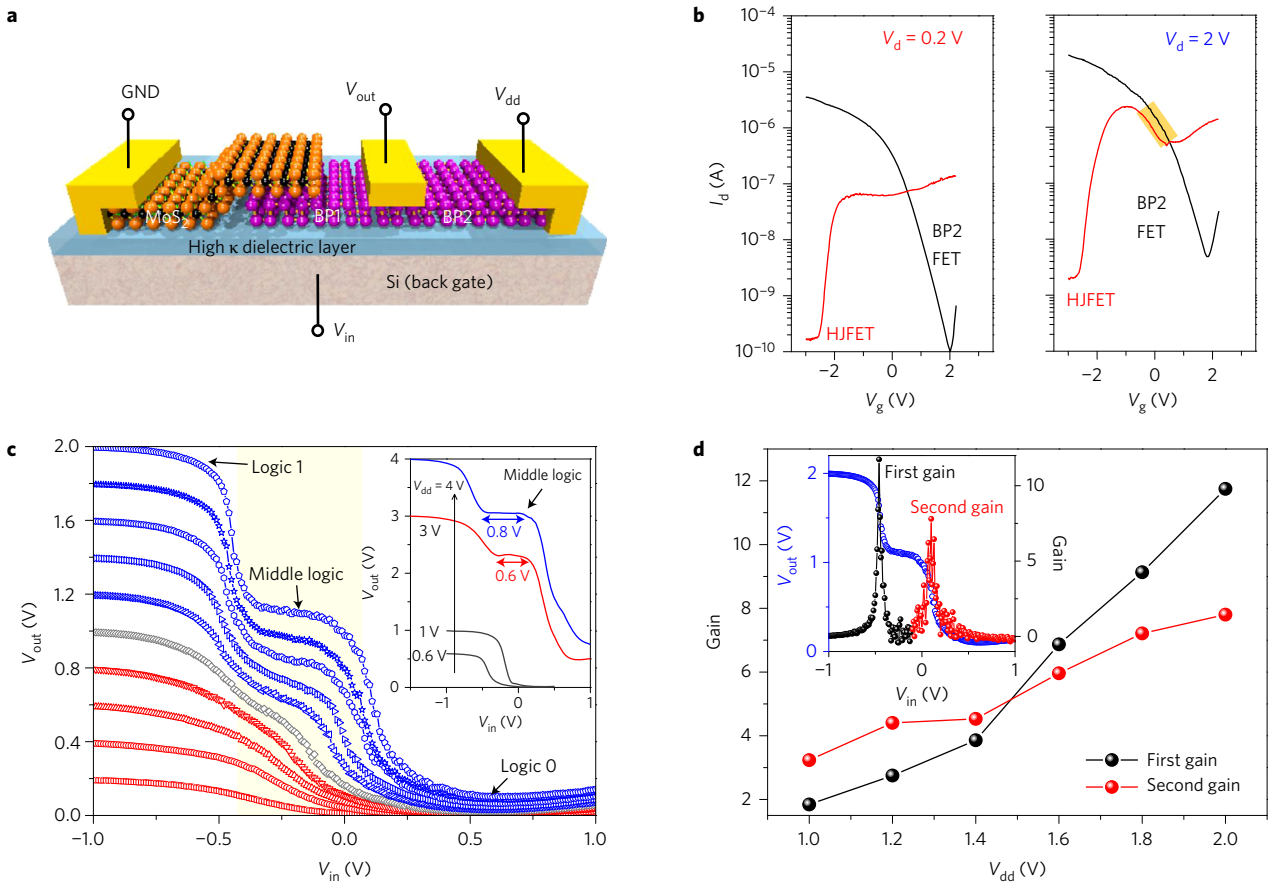
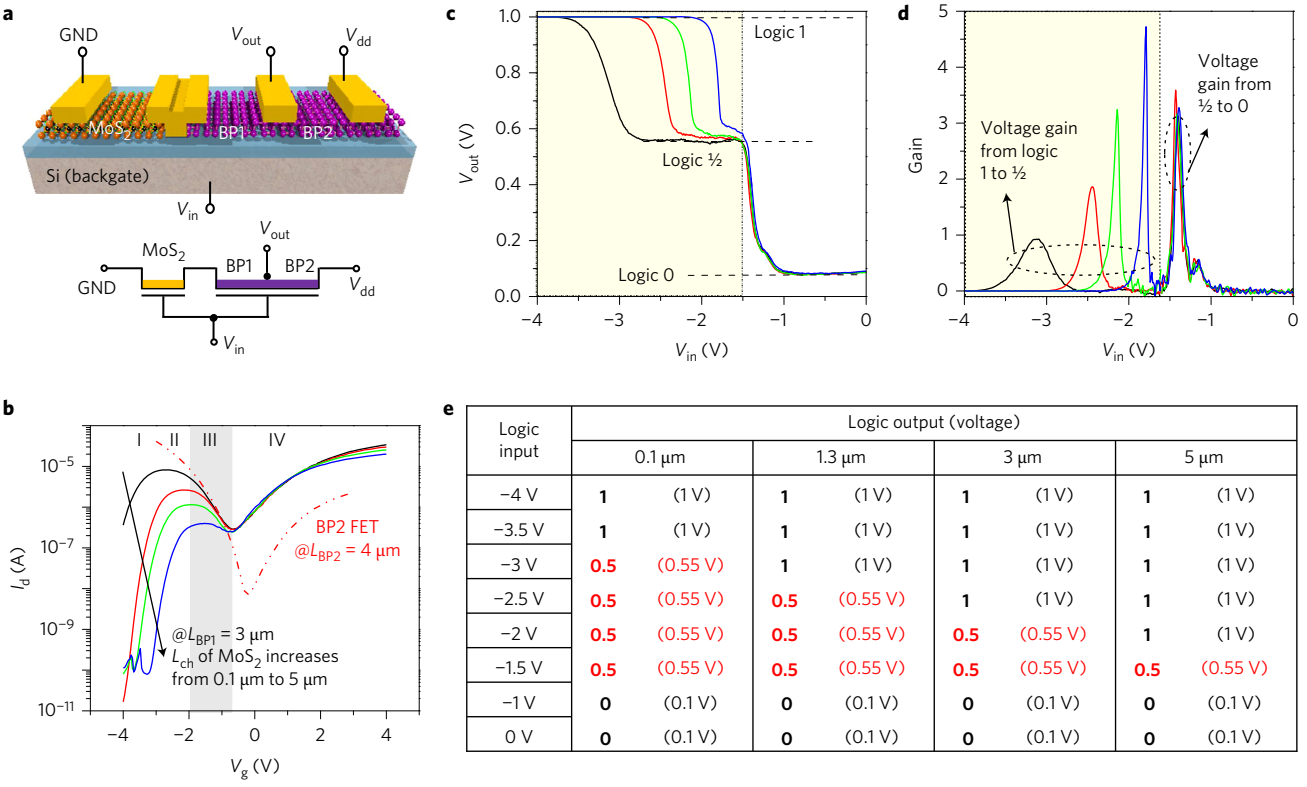


Figure 4 | Tunable multi-value inverter. a, Schematic view of the heterojunction-based ternary inverter. **b**, Transfer characteristics of the BP FET and lateral HJFET at small drain bias of 0.2 V (left) and large drain bias of 2 V (right), showing overlapped regions increasing at larger drain biases. **c**, Inverter formed by a BP FET and lateral HJFET showing binary logic under a small driving voltage and ternary logic under a large driving voltage; V_{dd} varies from 0.2 V to 2 V and the inflection point is ~1 V. Inset: another ternary inverter biased at 4 V with large mid-logic window. **d**, Voltage gain for both switching states for the ternary inverter at different V_{dd}. Inset: typical voltage gain dependence of V_{in}.

and MoS_2 transistor, where current in the depleted BP channel begins to decrease more quickly than the increase in MoS_2, until it reaches the ambipolar transition point when the current for both channels starts to increase beyond $V_g = 0$ V.

The energy band diagrams of this heterojunction under various biases are shown in Fig. 3c[28,29]. Under forward bias, the energy band of the BP side will be pulled down. The barrier for electrons in MoS_2 is always very small close to ohmic contact, and the barrier for holes in BP is large when V_d is small. When V_d increases further until the valence band of BP is pulled down beyond the valence band position of MoS_2 (at about $V_d = 1$ V), the barrier for holes decreases to zero and the BP channel will dominate current transport. The larger the drain bias, the more effectively the gate field controls the channel, where no internal barrier exists to restrain carrier transport. This explains the larger peak-to-valley ratio and faster decrease in current as V_d increases in region III, as shown in Fig. 3d (Supplementary Section 2). At large drain biases, the change in threshold voltage of the BP channel as well as the drain-induced barrier lowering[21] (which in this case also increases the subthreshold slope of the BP) lead to much larger parallel regions of this heterojunction and the BP channel, and this creates a unique window for a ternary logic inverter, as discussed in detail in Fig. 4.

Logic functions based on 2D semiconductors form building blocks with great potential for future flexible electronics[31–41]. Figure 4a shows an in-series lateral HJFET with a BP FET-based inverter. At small drain bias, the transfer characteristics of the heterojunction and BP transistor diverge widely, with very different gate voltage dependences, as shown in the left panel of Fig. 4b. However, at large drain bias, the peak-to-valley ratio of the heterojunction increases in region III, and forms a wide parallel region with the BP channel in the transfer characteristics shown in the right panel of Fig. 4b. As a result, the device shows binary logic under small driving voltage but ternary logic under large V_{dd}, as shown in Fig. 4c. For example, at $V_{dd} = 0.2$ V, the output voltage shows a high logic value of 1 before −0.5 V and a low logic of 0 at $V_{in} > 0$ V. At $V_{dd} = 2$ V, in addition to 'logic 1' at $V_{in} < -0.5$ V and 'logic 0' at $V_{in} > 0.5$ V, a new middle logic value of $V_{out} \sim 1.1$ V appears in the range of $-0.4\ \text{V} < V_{in} < 0$ V. At logic 1, the BP2 transistor in the pull-up network will provide a low resistive path to the supply voltage. At logic 0, the resistance of the heterojunction in the pull-down network is small enough that the logic low levels are almost equal to GND. The unique middle logic state starts to appear at about $V_{dd} = 1$ V and gradually becomes distinct when V_{dd} is larger than 1.6 V. As discussed earlier, this is because the heterojunction is fully turned on with effective gate control where a longer parallel region III exists for the two transfer characteristics curves at large V_d (for details see Supplementary Section 3). This parallel region of the BP2 FET and the lateral HJFET in the log-scale transfer characteristics indicates that the resistance ratio of the pull-up transistor and pull-down transistor is constant, so a middle logic state evolves in the V_{out}–V_{in} characteristics[15,41]. When V_{dd} increases further to 4 V for a similar structure, the middle logic region width increases gradually and becomes very



e

Logic input	Logic output (voltage)							
	0.1 μm		1.3 μm		3 μm		5 μm	
−4 V	1	(1 V)	1	(1 V)	1	(1 V)	1	(1 V)
−3.5 V	1	(1 V)	1	(1 V)	1	(1 V)	1	(1 V)
−3 V	0.5	(0.55 V)	1	(1 V)	1	(1 V)	1	(1 V)
−2.5 V	0.5	(0.55 V)	0.5	(0.55 V)	1	(1 V)	1	(1 V)
−2 V	0.5	(0.55 V)	0.5	(0.55 V)	0.5	(0.55 V)	1	(1 V)
−1.5 V	0.5	(0.55 V)	0.5	(0.55 V)	0.5	(0.55 V)	0.5	(0.55 V)
−1 V	0	(0.1 V)	0	(0.1 V)	0	(0.1 V)	0	(0.1 V)
0 V	0	(0.1 V)	0	(0.1 V)	0	(0.1 V)	0	(0.1 V)

Figure 5 | Tunable ternary inverter. a, Schematic of the ternary inverter based on a MoS_2 transistor with varying channel length in series with BP FETs. **b**, Transfer characteristics of the BP FET and in-series BP/MoS_2 FETs, in which the channel length of the MoS_2 FET changes from 0.1 to 5 μm and those of the BP1 and BP2 FETs are fixed at 3 and 4 μm, respectively, at a fixed V_d of 1 V. **c**,**d**, Plot of V_{out} versus V_{in} and voltage gain of the ternary inverter at V_{dd} = 1 V. **e**, Summary of output logic states of the inverter for different L_{ch} of the MoS_2 FET.

flat, as can be seen in the inset of Fig. 4c. It is important to note that the actual voltage drop on the heterojunction is V_{out} (not V_{dd}), which corresponds to the actual V_d in the I_d–V_g curves in Fig. 4b. To the best of our knowledge, this is the first multivalue inverter that can be tuned from binary to ternary using a drain bias. Moreover, these FETs show fast switching in gate modulation, leading to a high voltage gain in the inverters, thanks to the large specific capacitance of the high-κ dielectric HfSiO used, as shown in the inset of Fig. 4d. The gain increases with V_{dd}, and the switching gains of the first and second logic states can reach up 12 and 8 at V_{dd} = 2 V, as shown in Fig. 4d. The high performance and versatility demonstrated here promise great potential for future logic applications based on 2D material heterojunctions (Supplementary Section 12).

In-series FET

The transfer characteristics of MoS_2 transistors with different channel lengths show that the threshold voltage decreases and transconductance increases when the channel length decreases[21,43]. With these characteristics in mind, a ternary inverter structure based on a MoS_2 transistor (with varying channel length) in series with a BP channel was fabricated, as shown in Fig. 5a. Unlike previous studies of a CMOS inverter based on a MoS_2 nFET and BP pFET, the BP channel was designed to be divided into two regions with a 1 μm difference in channel length. This leads to a small difference in the on-state resistance and orders of difference in the off-state resistance due to the threshold voltage shift. The transfer characteristics of the in-series MoS_2 FET with the BP FET are presented in Fig. 5b, with the channel length of the MoS_2 FET changing from 0.1 to 5 μm and those of the BP1 and BP2 FET fixed at 3 and 4 μm, respectively, at a fixed V_d of 1 V. Similar to the heterojunction, there are four regions in the I_d–V_g curve, with regions I/II and III/IV dominated by the MoS_2 FET and BP FET, respectively. Thus, by combining such an in-series FET with a long-channel BP FET, a standard ternary inverter has been successfully demonstrated, as shown in the plot of output voltage versus input voltage in Fig. 5c. The three logic states—logic 1, ½ and 0—can all be clearly observed. In such an in-series circuit, the current through each component is the same, and the voltage across the circuit is the sum of the voltages across each component. We take the red line (L_{ch} of MoS_2 is 1.3 μm) as an example, which also correlates with the red line data in Fig. 5b. When $V_{in} < -2.5$ V, it shows a high logic value of 1, because of the highly resistive fully depleted MoS_2 channel ($R_{MoS2} \gg R_{BP1} \sim R_{BP2}$). When -2.5 V $< V_{in} < -1.5$ V, the MoS_2 channel starts to turn on, with higher conductance than the rest of the channel, and it exhibits a medium value of $V_{out} \sim 0.55$ V, corresponding to a partition of voltage between the load BP2 FET and BP1 FET together with the MoS_2 FET. When $V_{in} > -1.5$ V, the MoS_2 transistor is fully turned on with much lower resistance, while both BP transistors are in the state of the subthreshold region of the pFET where the longer channel BP2 has much higher resistance than BP1, and the resulting V_{out} shows a low level of ~0.1 V. Therefore, we have three state output values that are all close to conventional logic values. Figure 5d plots the gain of the ternary inverter. The first four peaks represent the voltage gain from logic 1 to ½, and the second four peaks represent the voltage gain from logic ½ to 0. Under a small driving voltage of V_{dd} = 1 V, the two gains can both reach close to 4. The advantage of such a structure is that the mid value state can be well controlled by simply tuning the channel length without the need for a deterministic transfer of materials and complex doping schemes. As shown in Fig. 5e, the middle region width can be controlled by the channel length of the MoS_2 FET, which determines the transition point from logic 1 (Supplementary Sections 4 and 5).

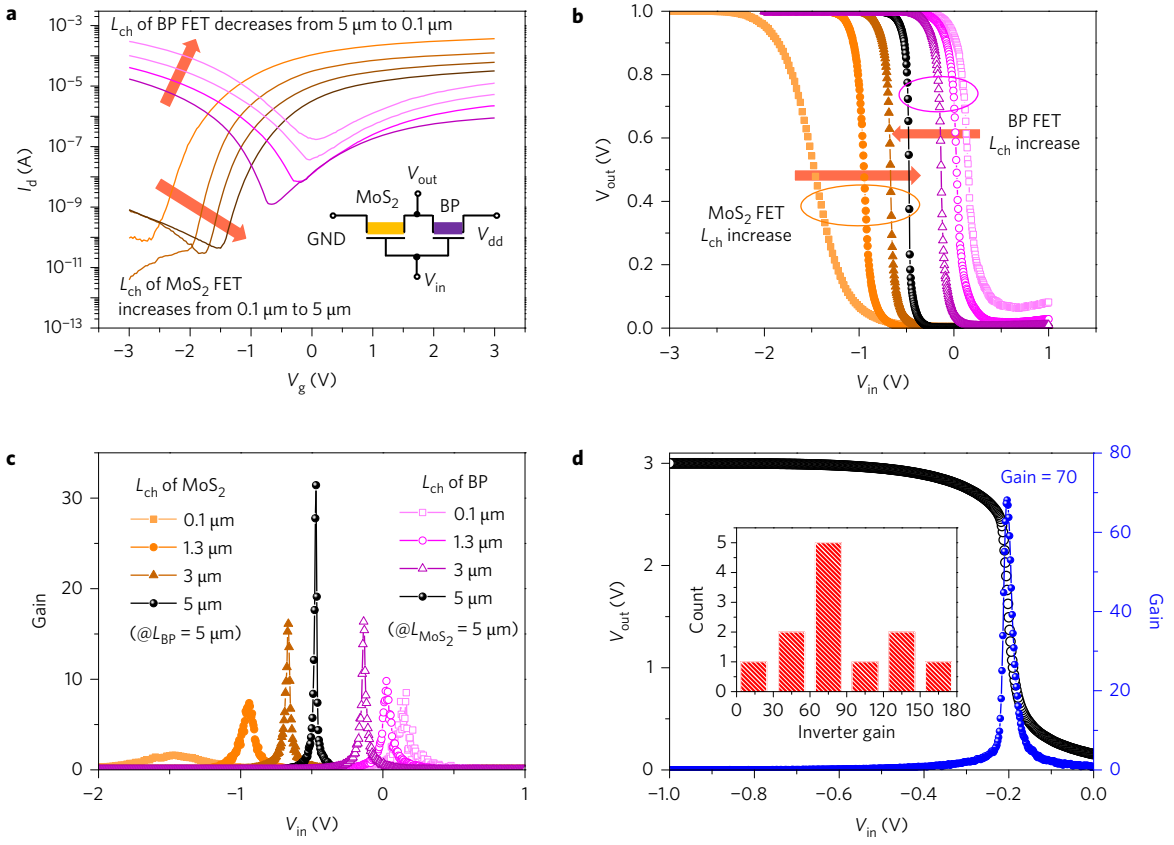


Figure 6 | High-performance binary inverter. a, Transfer characteristics of FETs with different channel lengths for BP and MoS_2. Inset: the circuit of the BP–MoS_2 binary inverter. **b**, V_{out} versus V_{in} for inverters based on BP and MoS_2 with different channel lengths. **c**, Voltage gain for the above inverters. **d**, High gain of the inverter based on an in-series BP FET (L_{ch} = 5 μm) and MoS_2 FET (L_{ch} = 5 μm). At V_{dd} = 3 V, the voltage gain can reach as high as 70. Inset: statistical distribution of the voltage gains from multiple devices. Five of the devices exhibit a gain of ~70, with a highest gain of over 150.

High-performance BP–MoS_2 binary inverter

Finally, to fully explore the performance potential of the BP/MoS_2-based logic inverter, arrays of BP and MoS_2 CMOS transistors with different channel lengths from 100 nm to 5 μm were fabricated in series, as shown in the inset of Fig. 6a. As expected, the threshold voltage can be well tuned by channel length modulation. We can make the intersection point of the two I_dV_g curves of the BP and MoS_2 FETs in their sub-threshold regions at an optimized channel length, resulting in a high-voltage-gain inverter, as shown in Fig. 6b,c. For an inverter with $L_{BP} = L_{MoS2} = 5$ μm, in particular, the small subthreshold slope of the MoS_2 FET (120 mV dec^{-1}) and the BP FET (245 mV dec^{-1}), together with their well-matched threshold voltages, leads to fast switching as the input voltage changes from 0 to −1 V. The gain can reach 31 at a small V_{dd} of 1 V (Fig. 6c) and 70 at V_{dd} = 3 V (Fig. 6d), which is comparable to commercial devices. We also fabricated 12 BP–MoS_2 CMOS inverters, for which the voltage gains are shown in the inset of Fig. 6d. Most of them exhibit high gains, larger than 60, and the highest gain is as high as 152 at V_{dd} = 3 V (Supplementary Section 6), which is among the highest reported in all inverters made from 2D materials, especially those that use solid-state gate oxide[38,40]. Finally, because BP is known for its air instability, we developed an encapsulation method with a thin Al_2O_3 layer, and the BP devices exhibit air-stable device performance for up to 8 weeks, with no sign of degradation (Supplementary Sections 7 and 8). We also carried out a temperature dependence study for the above functional devices, from room temperature down to 20 K (Supplementary Sections 7–11), and the performance of these devices improves at low temperatures. These multifunctional high-performance devices show great potential for future flexible electronics (Supplementary Section 13).

Conclusion

In summary, we have demonstrated various heterostructures based on 2D semiconductors with specific bandgap alignment, resulting in unique electronic transport properties and device performance. The vertically stacked MoS_2 and BP heterojunction exhibits a large current rectification ratio of 1×10^6 and high on–off ratio of 1×10^7 by integrating the high performance of the diode and FET into a single device. Tunable high-performance ternary inverters controlled by drain voltage and channel length have been demonstrated by adopting energy band alignment and load matching. Finally, a high-performance binary inverter with gain over 150 has been realized by optimization of the device structures of both 2D semiconductors.

Methods

Methods and any associated references are available in the online version of the paper.

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Author contributions

Y.W. conceived the project. M.H. transferred the heterostructures and fabricated the devices. M.H. and S.L. performed optical characterizations and electrical measurements. M.H., X.L. and Y.W. analysed the data. Z.Z. grew the CVD MoS_2 and X.X. grew the high-κ dielectric layers. M.H. and Y.W. co-wrote the paper. All authors contributed to discussions about the manuscript.

Additional information

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Competing financial interests

The authors declare no competing financial interests.

Methods

Fabrication of heterostructures. MoS_2 flakes were either transferred from a CVD-grown single layer or a mechanically exfoliated multilayer onto a silicon wafer with 20 nm high-κ dielectric grown by atomic layer deposition. Next, deterministic transfer methods were used to exfoliate few-layer BP onto the MoS_2. Finally, Ni/Au metal electrodes were patterned and deposited by standard electron-beam lithography and electron-beam deposition, respectively. Some heterostructures were based on monolayer CVD MoS_2 ribbons. The film was first patterned by electron-beam lithography and then etched into ribbons by oxygen plasma etching.

Electronic characterization. The device was placed inside an electrically shielded and optically sealed probe station system (Lakeshore CPX-VF). Current characterizations were carried out directly using an Agilent parameter analyser B1500A.

Data availability. The data that support the plots within this paper are available from the corresponding author upon reasonable request.